DATA SHEET

凌陽科技
SUNPLUS

SPLC100A2

40-Channel SEG/COM LCD Driver

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JUL. 09, 2002

Version 1.4

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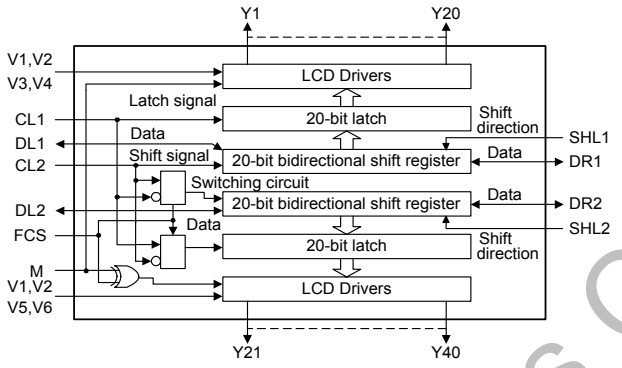
40-CHANNEL SEG/COM LCD DRIVER

1. GENERAL DESCRIPTION

The SPLC100A2 is a Liquid Crystal Display driver that contains two sets of 20-bit bi-directional shift registers, 20 data latch flip-flops and 20 Liquid Crystal Display drivers. It also features 40-channel outputs that can be applied as common or segment driver. The SPLC100A2 receives serial display data from a display control LSI, converts it into parallel data and supplies liquid crystal display waveforms to the liquid crystal.

2. BLOCK DIAGRAM



3. FEATURES

- Liquid Crystal Display driver with serial/parallel conversion function.
- Serial transfer facilitates board design.
- Capable of interfacing to liquid crystal display controllers: HD43160AH, HD61830, HD44780, HD44790, SPLC780
- 40 internal LCD drivers.
- Internal serial/parallel conversion circuits:
  - — 20-bit shift register × 2
  - — 20-bit latch × 2
- Power supply:
  - — Internal logic: 2.7V - 5.5V
  - — Liquid crystal display driver circuit: 3.0V - 11V
- CMOS process.
- Package form: 64 QFP or bare chip available

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4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
VDD	22	I	Positive power supply voltage input
VSS	32	I	Ground input
VEE	29	I	Power supply voltage for liquid crystal display drive
Y1 - Y6 Y7 - Y20	28 - 23 21 - 8	O	Liquid crystal driver output (Channel 1)
Y21 - Y27 Y28 - Y40	7 - 1 59 - 47	O	Liquid crystal driver output (Channel 2)
V1, V2	41, 42	I	Power supply for liquid crystal display drive (Select level)
V3, V4	43, 44	I	Power supply for liquid crystal display drive (Non-select level for channel 1)
V5, V6	45, 46	I	Power supply for liquid crystal display drive (Non-select level for channel 2)
SHL1	38	I	Selection of the shift direction of channel 1 shift register SHL1 / DL1 / DR1 VDD / Out / In GND / In / Out
SHL2	39	I	Selection of the shift direction of channel 2 shift register SHL2 / DL2 / DR2 VDD / Out / In GND / In / Out
DL1, DR1	33, 34	I/O	Data Input / Output of channel 1 shift register
DL2, DR2	35, 36	I/O	Data Input / Output of channel 2 shift register
M	37	I	Alternated signal for liquid crystal driver output
CL1	30	I	Latch signal for channel 1 ( ) *1 Used for channel 2 when FCS is GND
CL2	31	I	Shift signal for channel 1 ( ) *1 Used for channel 2 when FCS is GND
FCS	40	I	Mode select signal of channel 2. FCS signal exchanges the latch signal and the shift of channel 2 and inverts M for channel 2.Thus, this signal exchanges the function of channel 2. FCS Level / Channel 2 (Latch signal, Shift signal) / M Polarity / Function VDD / CL2 / CL1 / M / For common drive GND / CL1 / CL2 / M / For segment drive *1 *1 *2

Note: *1. and indicate the latches at rise and fall times, respectively.

Note: *2. The output level relationship between channel 1 and channel 2 based on the FCS signal level as follows:

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FCS	Data	M	Output Level	
			Channel 1(Y1 - Y20)	Channel 2(Y21 - Y40)
VDD (H)	H (Select)	H	V1	V2
		L	V2	V1
	L (Non-select)	H	V3	V6
		L	V4	V5
GND (L)	H (Select)	H	V1	V1
		L	V2	V2
	L (Non-select)	H	V3	V5
		L	V4	V6

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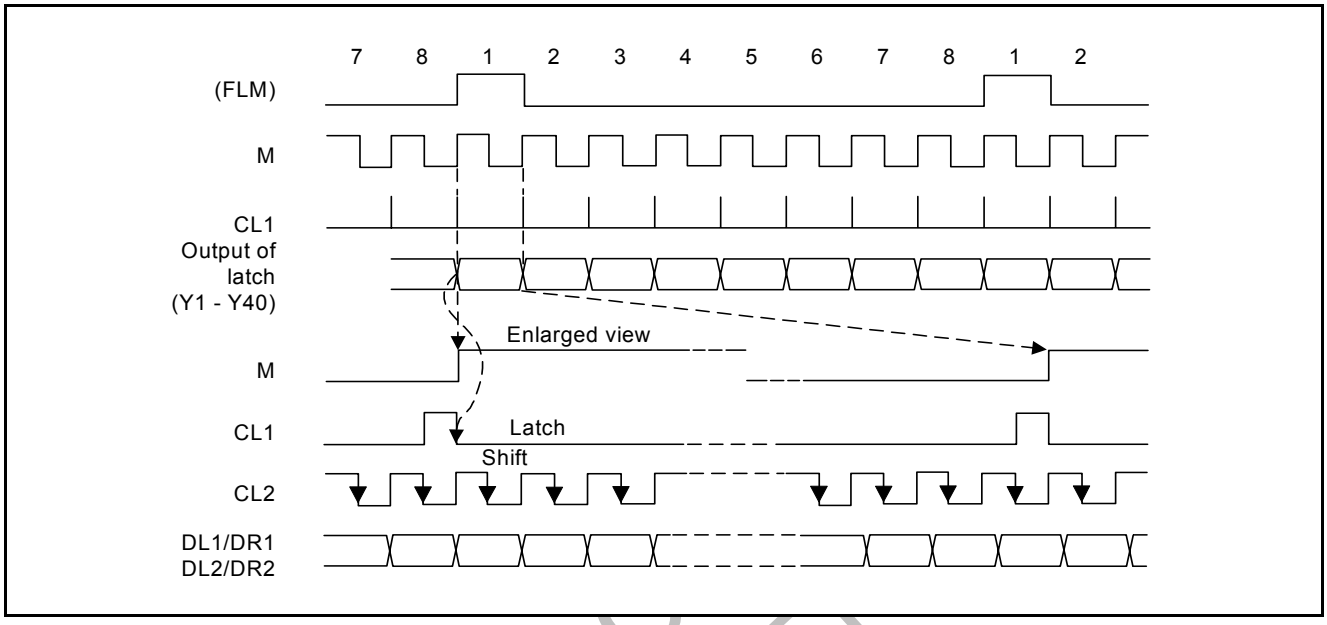
5. FUNCTIONAL DESCRIPTIONS

5.1. Segment Driver

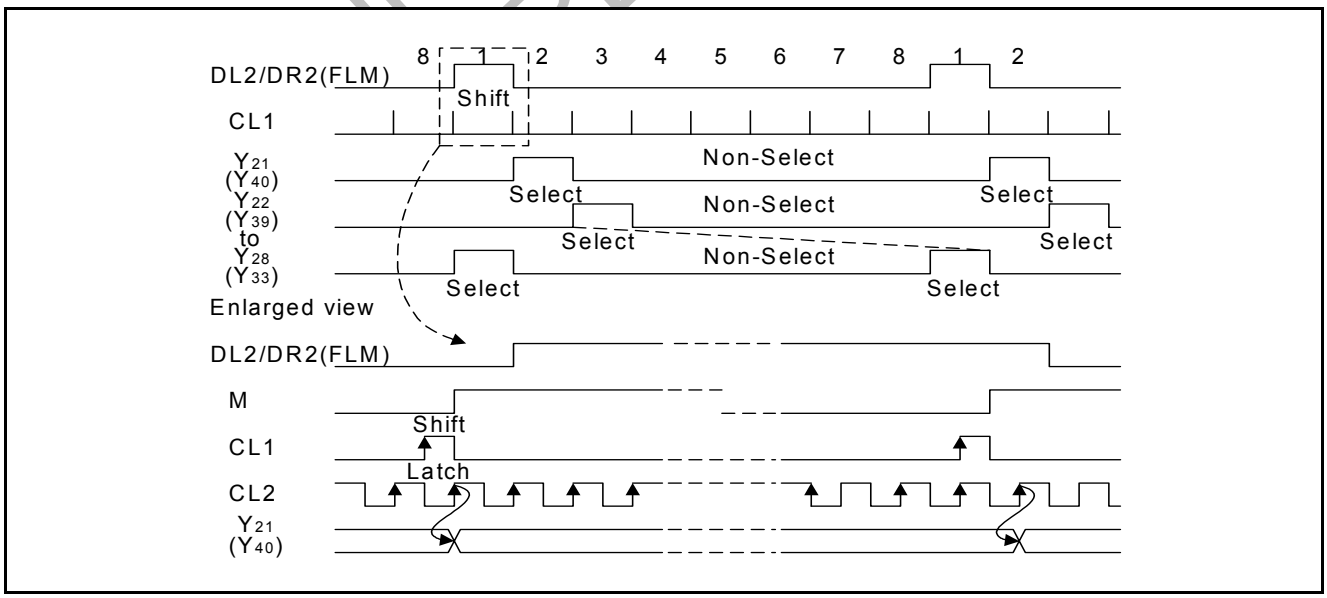
When SPLC100A2 is used as a segment driver, FCS is connected to VSS. In this case, both channel 1 and channel 2 shift data at the falling edge of CL2 and latch it at the falling edge of CL1. V3 and V5, V4 and V6 of the liquid crystal display driver power supply are short-circuited, respectively.



Segment data waveforms (A type waveforms, 1/8 duty cycle)

5.2. Common Driver

In this case, channel 1 is used as a segment driver and channel 2 as common driver. When channel 2 of SPLC100A2 is used as common driver, FCS is connected to VDD. In this case, channel 2 shifts data at the rising edge of CL1 and latches it at the rising edge of CL2.



Common data waveforms (A type waveforms of channel 2, 1/8 duty cycle)

5.3. Both Channel 1 and Channel 2 Used as Common Drivers (FCS = VSS)

5.3.1. Common drivers (FCS = VSS)

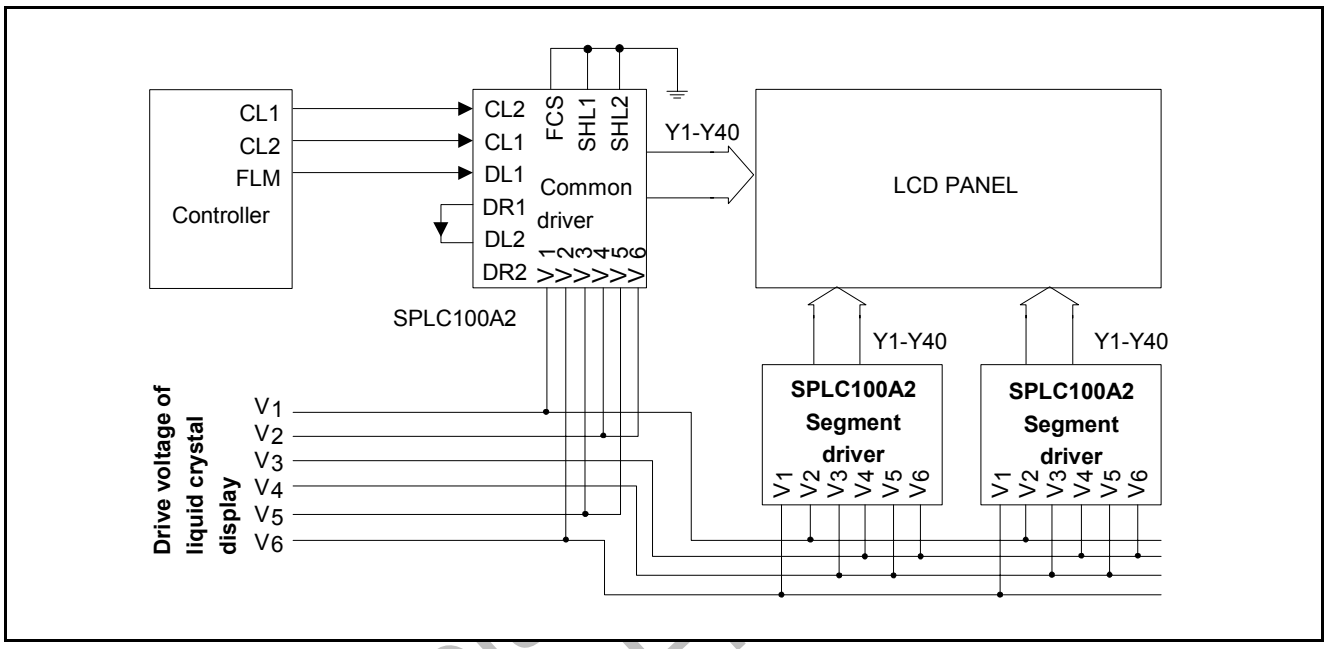
When both of channel 1 and channel 2 are used common drives, FCS is connected to VSS and the signals (CL1, CL2, FLM) from the controller are connected as following.

In this case, connection of the Liquid Crystal Display driver power supply is different from that of segment driver,

1). V1, V2: Select level of segment and common

2). V3, V4: Non-select level of segment

3). V5, V6: Non-select level of common



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6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
Operating Voltage	VDD *1	-0.3V to + 7.0V
LCD Driver Supply Voltage	VEE *2	VDD - 13.5V to VDD+ 0.3V
Input Voltage 1	V_{IN1}	-0.3V to VDD + 0.3V
Input Voltage 2 (V1 - V6)	V_{IN2}	VDD + 0.3V to VEE -0.3V
Operating Temperature	T_{OPR}	-20℃ to + 75℃
Storage Temperature	T_{STG}	-55℃ to + 125℃

Note1: It will cause damage to IC if the supply voltage is greater than above.
Note2: Connect a protection resistor of 220Ω±5% to VEE.
Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. DC Characteristics

(VDD = 2.7V - 5.5V, VDD - VEE = 3.0V - 11V , VSS = 0V, T_A = +25℃)

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Voltage (CL1, CL2, DL1, DL2, DR1, DR2, M, SHL1, SHL2, FCS)	V_{IH}	0.7VDD	-	VDD	V	
	V_{IL}	0	-	0.3VDD	V	
Output Voltage (DL1, DL2, DR1, DR2)	V_{OH}	VDD-0.4	-	-	V	I_{OH} = -0.1mA
	V_{OL}	-	-	0.4	V	I_{OL} = +0.1mA
LCD Driver Voltage	V_{LCD}	3.0	-	11	V	VDD - V5
Vi-Yj Voltage Descending V(V1 - V6)-Y(Y1 - Y40)	V_{D1}	-	-	1.1	V	I_{ON} = 0.1mA for one of Yj
	V_{D2}	-	-	1.5	V	I_{ON} = 0.05mA for each Yj
Input Leakage Current (CL1, CL2, DL1, DL2, DR1, DR2, M, SHL1, SHL2, FCS)	I_{IL}	-5.0	-	5.0	μA	V_{IN} = 0 to VDD
Vi Leakage Current V1 - V6	I_{VL}	-10	-	10	μA	V_{IN} = VDD - VEE (Output Y1 - Y40: floating)
Power Supply Current	I_{CC}	-	-	1.0	mA	F_{CL2} = 400KHz
	I_{EE}	-	-	10	μA	F_{CL1} = 1.0KHz

6.3. AC Characteristics

Characteristics		Symbol	Min.	Typ.	Max.	Unit	Test Condition
Data Shift Frequency (CL2)		F_{CL}	-	-	400	KHz	
Clock Width	High Level (CL1, CL2)	t_{CWH}	800	-	-	ns	
	Low Level (CL2)	t_{CWL}	800	-	-	ns	
Data Set-up Time (DL1, DL2, DR1, DR2, FLM)		t_{SU}	300	-	-	ns	
Clock Set-up Time (CL1, CL2)		t_{SL}	500	-	-	ns	(CL2→CL1)
Clock Set-up Time (CL1, CL2)		t_{LS}	500	-	-	ns	(CL1→CL2)
Date Delay Time (DL1, DL2, DR1, DR2)		t_{PD}	-	-	500	ns	CL = 15pF
Clock Rise/Fall Time (CL1, CL2)		t_{CT}	-	-	200	ns	
Date Hold Time (DL1, DL2, DR1, DR2, FLM)		t_{DH}	300	-	-	ns	

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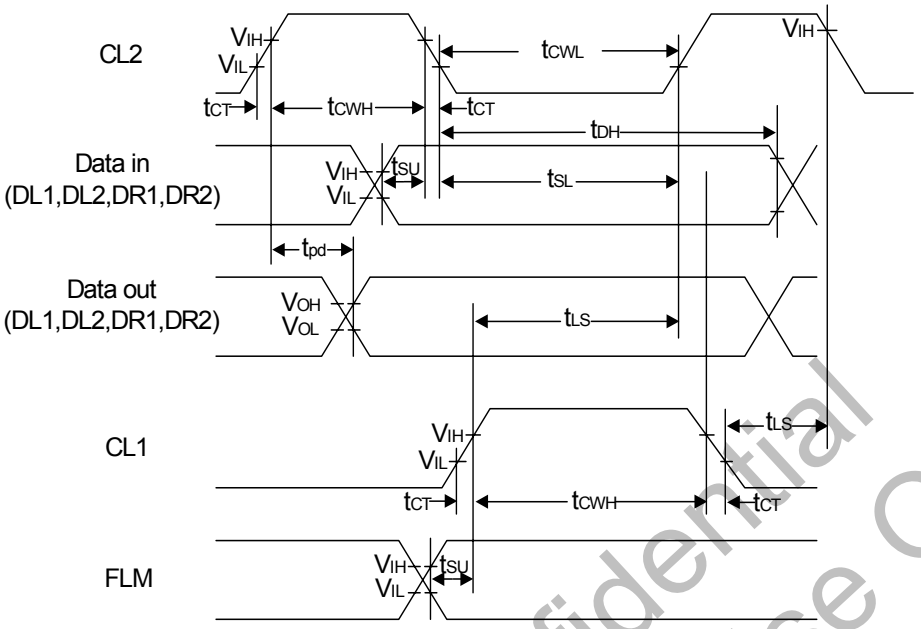

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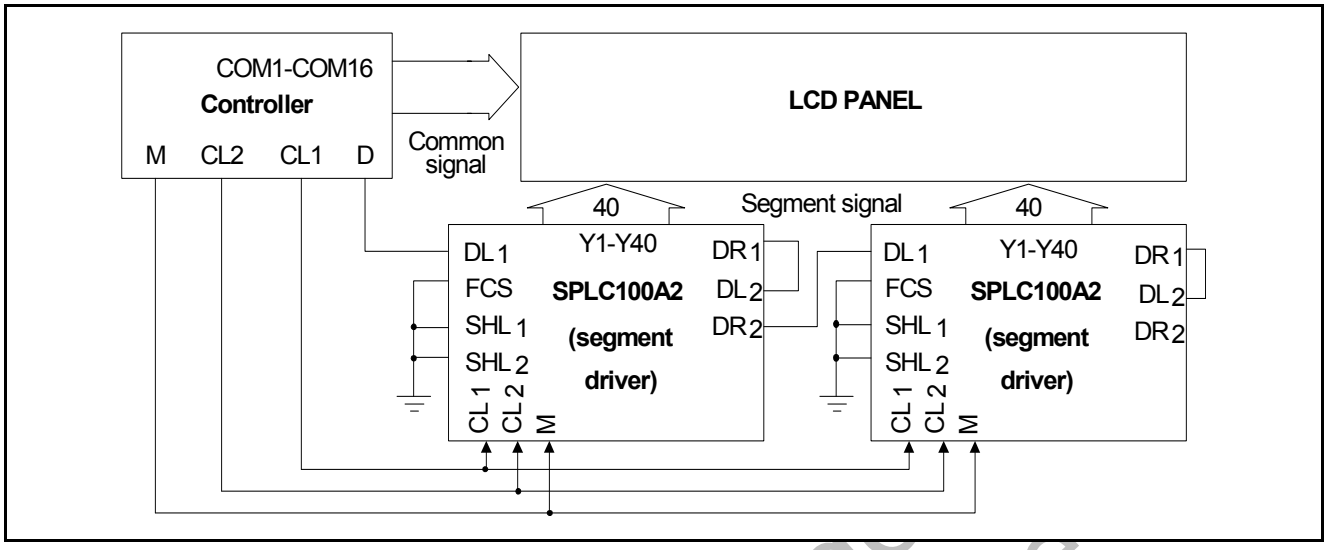
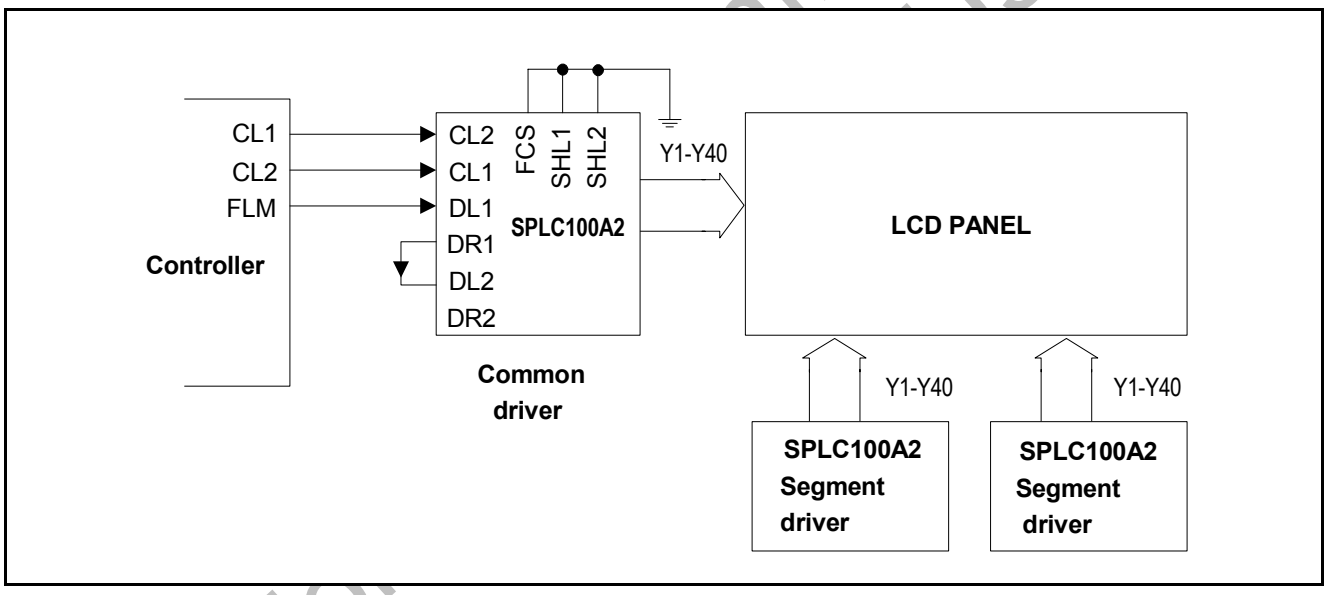
7. APPLICATION CIRCUITS

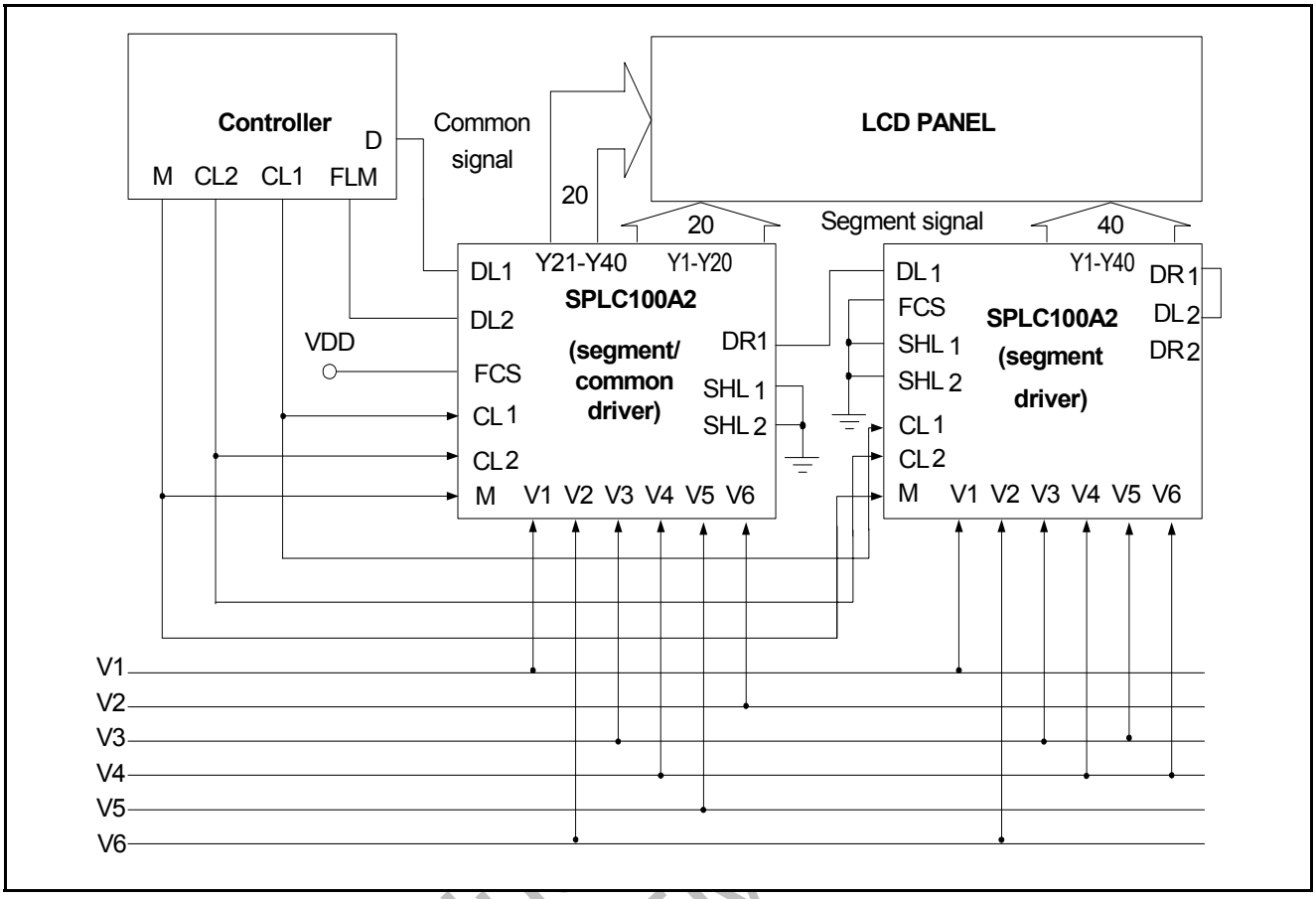
7.1. Segment Driver



7.2. Common Driver



7.3. Segment / Common Driver



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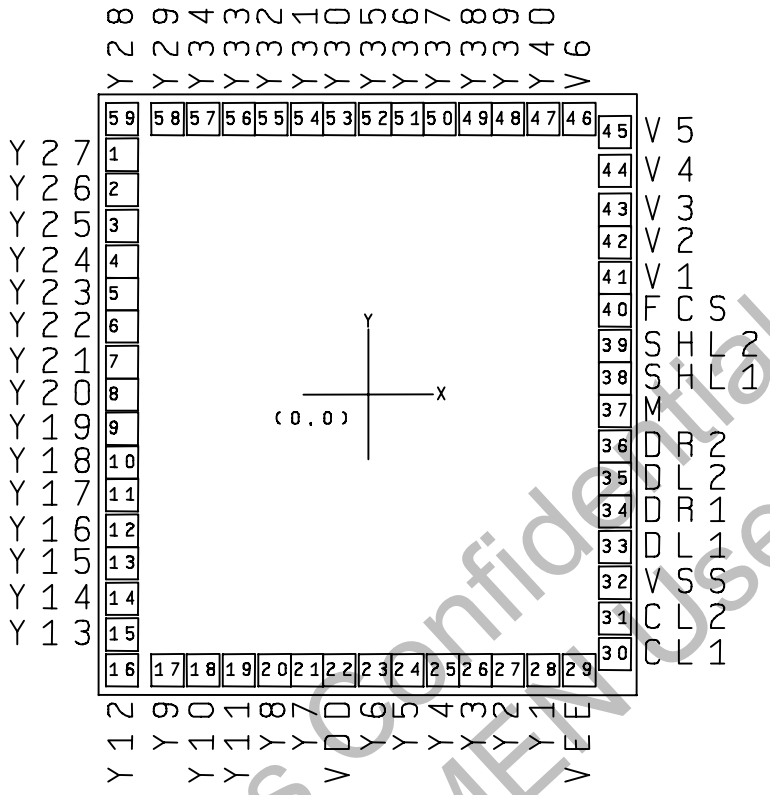
8. PACKAGE/PAD LOCATIONS

8.1. PAD Assignment



Chip Size: 2180μm x 2410μm

PAD Size: 96μm X 96μm

This IC substrate should be connected to VDD

Note1: Chip size included scribe line.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

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8.2. Ordering Information

Product Number	Package Type
SPLC100A2-nnnnV-C	Chip form
SPLC100A2-nnnnV-PQ04	Package form - QFP 64L

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (V = A - Z).

8.3. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	Pad Name	X	Y
1	Y27	-888	837	31	CL2	883	-817
2	Y26	-888	716	32	VSS	883	-690
3	Y25	-888	595	33	DL1	883	-566
4	Y24	-888	474	34	DR1	883	-442
5	Y23	-888	352	35	DL2	883	-319
6	Y22	-888	231	36	DR2	883	-195
7	Y21	-888	110	37	M	883	-72
8	Y20	-888	-10	38	SHL1	883	51
9	Y19	-888	-132	39	SHL2	883	175
10	Y18	-888	-253	40	FCS	883	298
11	Y17	-888	-374	41	V1	883	422
12	Y16	-888	-495	42	V2	883	546
13	Y15	-888	-616	43	V3	883	669
14	Y14	-888	-738	44	V4	883	798
15	Y13	-888	-859	45	V5	883	934
16	Y12	-888	-992	46	V6	754	998
17	Y9	-748	-1000	47	Y40	621	998
18	Y10	-622	-1000	48	Y39	489	998
19	Y11	-496	-1000	49	Y38	366	998
20	Y8	-370	-1000	50	Y37	242	998
21	Y7	-244	-1000	51	Y36	118	998
22	VDD	-111	-1023	52	Y35	-4	998
23	Y6	18	-1000	53	Y30	-128	998
24	Y5	138	-1000	54	Y31	-252	998
25	Y4	258	-1000	55	Y32	-375	998
26	Y3	378	-1000	56	Y33	-499	998
27	Y2	498	-1000	57	Y34	-622	998
28	Y1	618	-1000	58	Y29	-746	998
29	VEE	751	-1023	59	Y28	-888	998
30	CL1	883	-944				

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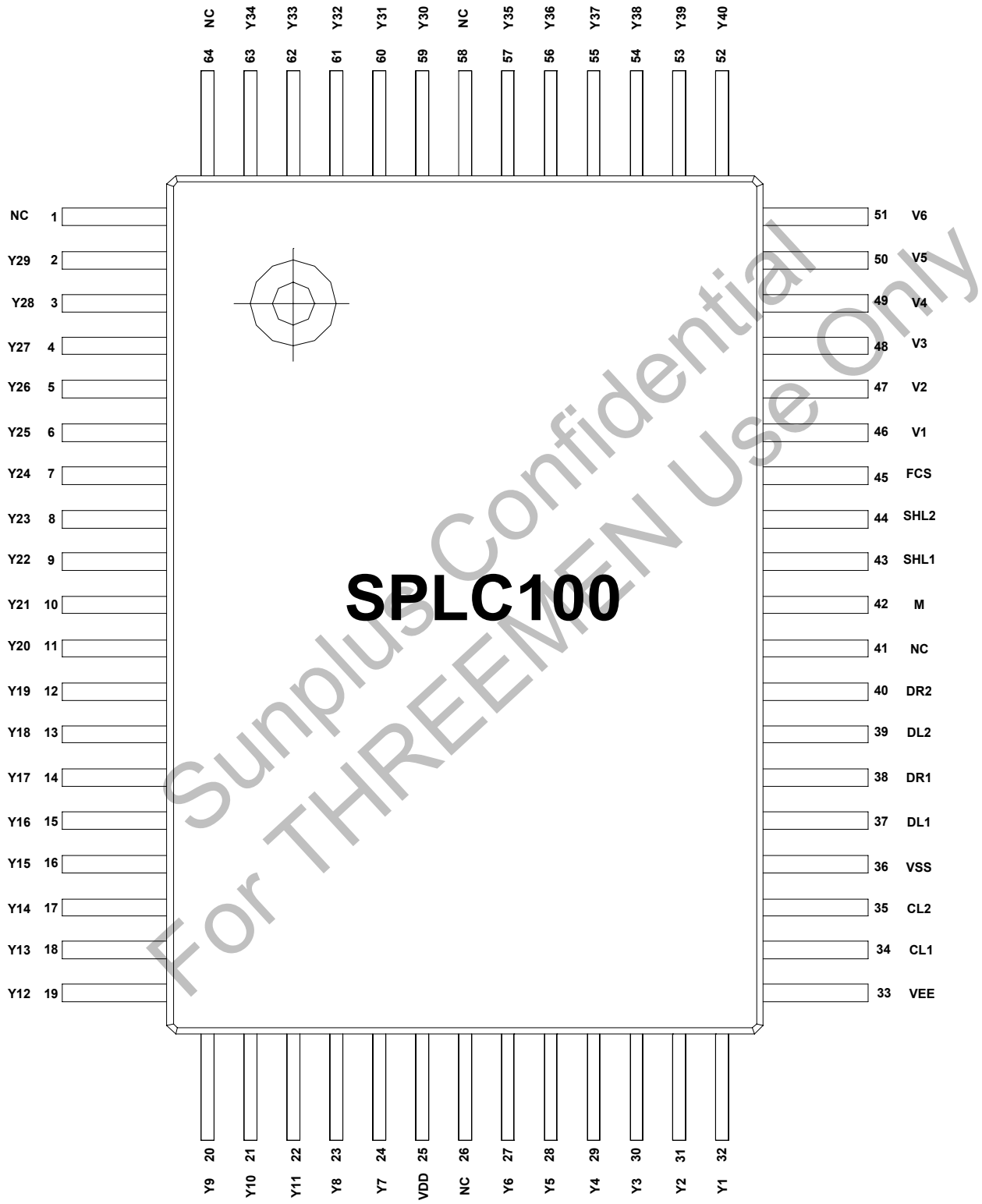
8.4. Package Configuration

QFP 64L Top View



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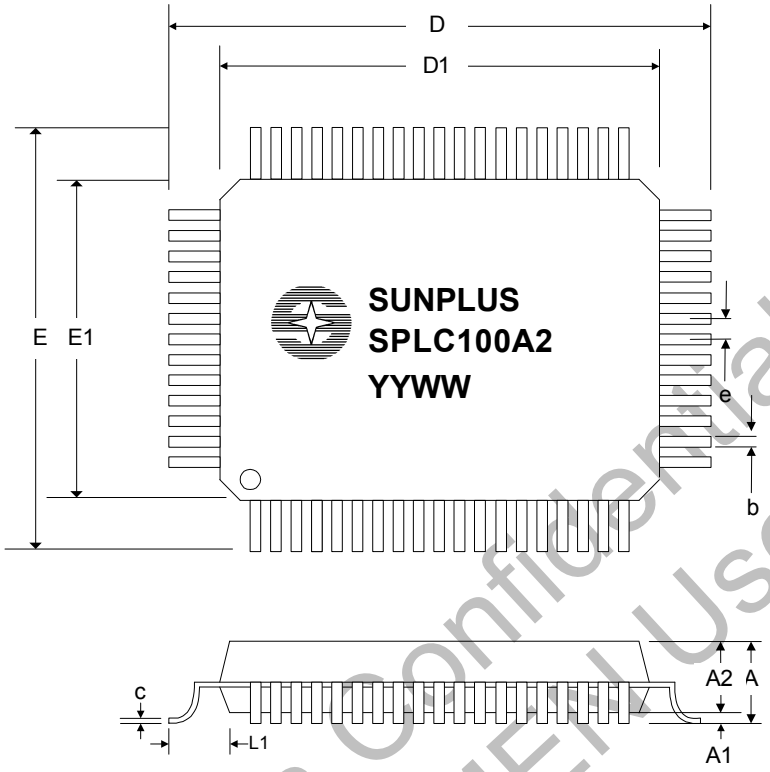
8.5. Package Information

QFP 64L Outline Dimensions

Unit: Millimeter



Symbol	Min.	Nom.	Max.	Unit
D		23.20 REF		Millimeter
D1		20.00 REF		Millimeter
E		17.20 REF		Millimeter
E1		14.00 REF		Millimeter
e		1.00 REF		Millimeter
b	0.35	0.40	0.50	Millimeter
A	-	-	3.40	Millimeter
A1	0.25	-	-	Millimeter
A2	2.50	2.72	2.90	Millimeter
c	0.11	0.15	0.23	Millimeter
L1		1.60 REF		Millimeter

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10. REVISION HISTORY

Date	Revision #	Description	Page
MAY. 05, 2000	0.1	Original	
OCT. 25, 2000	1.0	1. Delete "*PRELIMINARY*" 2. Modify Operating Current 3. Modify the pin sequence of COM/SEG in application circuit to the same as the LCD panel sequence 4. Add PAD size description	
MAY. 03, 2001	1.1	1. Correct chip size and PAD size in the "*8.1 PAD Assignment*" 2. Correct "*8.2 Ordering Information*" 3. Renew to a new document format	12 12
JAN. 30, 2002	1.2	1. Correct FCS signal in the *"5.3 Both Channel 1 and Channel 2 Used as Common Drivers"* 2. Correct FCS signal in the *"7.2 Common Driver Application Circuit"* 3. Redefine "Product Number" in the "*8.2 Ordering Information*"	7 10 12
MAY. 27, 2002	1.3	1. Correct "*5.2 Common Driver*" 2. Add description of controller's signal for "*5.3.1 Common drivers*" 3. Correct controller's CL1 and CL2 signal for "*7.2 Common Driver*" 4. Renew application circuit for "*7.3 Segment / Common Driver*"	6 7 10 11
JUL. 09, 2002	1.4	Update "*8.5 Package Information*"	15

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